control gate.

7. (Amended) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical floating gate [having sub lithographic dimensions] separated from a first portion of the channel region by a first oxide thickness; [and]

at least one edge-defined vertical control gate [having sub lithographic dimensions] separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate; and

wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate.

14. (Amended) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate [having sub lithographic dimensions] located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate [having sub lithographic dimensions] located above a second portion of the channel region and separated from the channel region by a second oxide thickness; [and]

a third edge-defined vertical gate [having sub lithographic dimensions] located above a third portion of the channel region and separated from the channel region by the second oxide thickness; and

wherein a first capacitance associated with one of the vertical gates is smaller than a second capacitance associated with the remaining vertical gates.